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Please add the following new claims:

--19. The semiconductor device of claim 1, further comprising at least one test pin corresponding to said at least one test pad for applying a positive or negative voltage to said at least one test pad.

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20. The semiconductor device of claim 1, further comprising at least one test pin corresponding to said at least one test pad for detecting a voltage or a current from said at least one test pad.--

REMARKS

It is respectfully submitted that the amendment to the specification and drawings overcome the Examiner's objections to the specification. Accordingly, it is respectfully requested that the objection to the specification be withdrawn.

Claims 1 and 3-5 stand objected to for minor informalities. In order to expedite prosecution, claims 4 and 5 have been amended as kindly suggested by the Examiner with respect to those claims. However, it is respectfully submitted that the term "chip IP" is correct as currently written and that one of ordinary skill in the art would readily understand the meaning of the term as understood in the art. Based on the foregoing, it is respectfully requested that the objection to claims 1 and 3-5 be withdrawn.

I. CLAIMS 1 AND 3 ARE NOT ANTICIPATED BY NAKANISHI ET AL.

Claims 1 and 3 stand rejected under 35 U.S.C. § 102 over Nakanishi et al.. Claim 1 is independent. This rejection is respectfully traversed for the following reasons. The

Examiner alleges that the test pad 3 "is inherently capable of functioning as a test pad ... ." However, even assuming *arguendo* true, such an allegation does not render Nakanishi et al. anticipatory of claim 1. As is well known in patent prosecution, anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently, in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986). As further well known, "inherency may not be established by probabilities or possibilities," *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999).

Accordingly, a proper rejection under § 102 requires that each and every claim limitation ***necessarily*** be disclosed in a single prior art reference. That is, the alleged test pad 3 of Nakanishi et al. MUST function "for testing an electrical connection between the circuit of the chip IP and the wires" as recited in claim 1. The alleged fact that test pad 3 is "capable" of functioning in the manner recited in claim 1 is not relevant to the determination of patentability under § 102. As implicitly admitted by the Examiner, the test pads 3 of Nakanishi et al. are <u>not</u> arranged/configured to test electrical connections, let alone ***necessarily*** function to test the electrical connection between the chips 1,1' and the wiring of substrates 17,18. Accordingly, Nakanishi et al. does not anticipate claims 1 and 3 under § 102.

Moreover, as described in Applicants' specification, testing the electrical connection of a chip circuit and wiring substrate can require more than just a test pad. For example, in one embodiment, voltage sources can be applied to ***two*** specifically arranged test pads, connected ***to and from*** the circuit, via respective test pins (one for applying voltage and one for detecting) so as to measure subsequent current flow

between the wires and the circuit (e.g., through a diode as shown in Figure 3A; *see, e.g.,* claim 4). In contrast, Nakanishi et al. discloses only that the test pads 3 serve as an intermediary for signals sent between chips 1,1' (*see, e.g.,* col. 6, lines 31-40). Nakanishi et al. is completely silent as to how the alleged test pads 3 would be used to test electrical connections between the substrate wiring and the chips, and certainly does not anticipate such a functionality. The Examiner has not established that the arrangement and connections of test pads 3 are adequate to perform testing, let alone ***necessarily*** function to perform testing.

In fact, there is no objective evidence that Nakanishi et al. needs or desires a testing functionality. For example, Nakanishi et al. does not disclose having a relatively large number of chip IPs as would be understood in the art such that reliable connections between the chip and wiring substrate are not as important. As such, it is respectfully submitted that there is no need for providing a quick and easy testing mechanism as can be done in the present invention (*see, e.g.,* page 2, line 24 - page 3, line 2 of Applicants' specification).

Regarding claim 3, the Examiner merely alleges that the test pad 3 of Nakanishi et al. "is a portion of the at least one of the wires ... ." However, none of the test pads 3 of Nakanishi et al. appear to be formed of wires in the substrates 17,18 and none of the wires of Nakanishi et al. appear to form part of test pads 3. Rather, Nakanishi et al. appears to disclose only that wires of the substrates are connected to the pads 3.

Based on all the foregoing, it is submitted that claims 1 and 3 are patentable over Nakanishi et al.. Accordingly, it is respectfully requested that the rejection of claims 1 and 3 under 35 U.S.C. § 102 be withdrawn.

II. CLAIMS 4 AND 5 ARE PATENTABLE OVER NAKANISHI ET AL. IN VIEW OF VOLDMAN

Claims 4 and 5 stand rejected under 35 U.S.C. § 103 over Nakanishi et al. in view of Voldman ('280). This rejection is respectfully traversed for the following reasons. Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination recited in claim 1.

For example with respect to claims 4 and 5, as discussed above, Nakanishi et al. does not disclose testing the electrical connections, let alone how to use pads 3 in a testing operation. Accordingly, there is no need or desire for providing the diode of Voldman in the circuit of Nakanishi et al. in the manner set forth by the Examiner, rendering the proposed modification without the requisite motivation/rationale from the prior art. It is respectfully submitted that the Examiner simply selected pieces of different prior art and relied solely on improper hindsight reasoning to reconstruct the claimed invention using only Applicants' specification as a guide. At best, the Examiner has attempted to show only that the ***individual*** elements of the claimed invention are known without providing a *prima facie* showing of obviousness that the ***combination*** of elements is known or suggested.

In particular, it is submitted that the proposed combination is improper because the Examiner has not provided the requisite ***objective*** evidence ***from the prior art*** that "suggests the desirability" of the proposed combination. As is well known in patent law, a *prima facie* showing of obviousness can only be established if the prior art "suggests the desirability" of the proposed combination using ***objective*** evidence. The Examiner is directed to MPEP § 2143.01 under the subsection entitled "Fact that References Can Be Combined or Modified is Not Sufficient to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. (*In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990)).

In the instant case, even assuming *arguendo* that Nakanishi et al. can be modified by Voldman, it is submitted that the "mere fact that [Nakanishi et al. in view of Voldman] can be combined ... does not render the resultant combination obvious" because nowhere does the ***prior art*** "suggest the desirability of the combination" as set forth by the Examiner.

The Examiner is further directed to MPEP § 2143.01 under the subsection entitled "Fact that the Claimed Invention is Within the Capabilities of One of Ordinary Skill in the Art is Not Sufficient by Itself to Establish *Prima Facie* Obviousness", which sets forth the applicable standard:

> A statement that modifications of the prior art to meet the claimed invention would have been [obvious] because the references relied upon teach that all aspects of the claimed invention were ***individually*** known in the art is ***not*** sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. (citing *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993)).

In the instant case, even assuming *arguendo* that Nakanishi et al. in view of Voldman "teach that all aspects of the claimed invention [are] individually known in the art", it is submitted that such a conclusion "is not sufficient to establish a *prima facie* case of obviousness" because there is no ***objective*** reason on the record to combine the teachings of the cited prior art. In contrast, Nakanishi et al. and Voldman are completely silent as to suggesting the ***combination*** of elements recited in the pending claims.

Based on all the foregoing, it is submitted that claims 4 and 5 are patentable over Nakanishi et al. in view of Voldman. Accordingly, it is respectfully requested that the rejection of claims 4 and 5 under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
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APPENDIX

IN THE SPECIFICATION

The paragraph beginning on page 11, line 10 has been amended as follows:

--FIG.'s **3A** and **3C** are [is a] block circuit diagrams illustrating a first testing method for testing the connection between an IP (chip IP) and wiring according to the first embodiment.--

The paragraph beginning on page 11, line 13 has been amended as follows:

--FIG.'s **3B** and **3D** are [is a] block circuit diagrams illustrating a second testing method for testing the connection between an IP (chip IP) and wiring according to the first embodiment.--

The paragraph beginning on page 15, line 1 has been amended as follows:

--A feature of the present embodiment is the provision of test pads **27**, **28**, **33** and **34** connected respectively to the wires **25**, **26**, **31** and **32**, which are connected to the circuit of the IP **24** whose electrical connection is to be tested. The wires **25**, **26**, **31** and **32** are provided in the form of the wiring layers **13** and **14** as illustrated in FIG. **1C**, and the test pads **27**, **28**, **33** and **34** are connected respectively to the wires **25**, **26**, **31** and **32** via contacts. The wire **25** is connected to a node **43a** of the circuit connected to an internal circuit **43** in the IP **24**, and the wire **26** to a ground line **41** in the IP **24**. The wire **31** is connected to a power supply line **42** in the IP **24**, and the wire **32** to a node [**43a**] **43b** of the internal circuit **43** in the IP **24**.--

The paragraph beginning on page 16, line 23 and ending on page 17, line 9, has been amended as follows:

--As illustrated in FIG. **3C**, when [When] testing the electrical connection between the wires **25** and **26** and the IP **24**, a positive voltage is applied from a test pin **36** via the test pad **28** to the ground line **41** in the IP **24**. If the electrical connection is good, a forward current flows, by a forward voltage, from a protection diode to a node **43a** of the internal circuit **43** of the IP **24** [to a protection diode]. Therefore, by detecting a current or by detecting a voltage according to a voltage drop using a test pin **35**, it is possible to determine the condition of the electrical connection between the IP and the wire in the silicon wiring substrate (for example, the condition of the connection between pads shown by broken lines in the figure) based on the measured voltage or current value.--

The paragraph beginning on page 17, line 12 and ending on page 18, line 9, has been amended as follows:

--FIG. **3B** is a block circuit diagram illustrating a second testing method for testing the connection between an IP (chip IP) and wiring. As illustrated in the figure, a selector **44** is provided in the IP **24**. The selector **44** receives, and selectively outputs one of, the output of the internal circuit **43** of the IP **24** and a power supply voltage VDD (ground voltage VSS), which is the output of the power supply line **42** (the ground line **41**). When testing the electrical connection between the wires **31** and **32** and the IP **24**, a logic voltage (e.g., H) such that the output of the power supply line **42** is selected is supplied to the selector **44** from the wire **32** via the test pad **34**. Then, if the electrical

connection is good, the power supply voltage VDD is output to the test pin **37** via the test pad **33**. Therefore, the condition of the electrical connection can be determined by measuring the voltage of the test pin **37**. As illustrated in FIG. **3D**, when [When] testing the electrical connection between the wires **25** and **26** and the IP **24**, a logic voltage (e.g., H) such that the output of the ground line **41** is selected is supplied to the selector **44** from the test pin **35** via the test pad **27**. Then, if the electrical connection is good, the ground voltage VSS is output to the test pin **36** via the test pad **28**. Therefore, the condition of the electrical connection can be determined by measuring the voltage of the test pin **36**.--

IN THE CLAIMS

4. (Amended) The semiconductor device of claim 1, wherein:

the circuit of the chip IP includes a power supply line for supplying a power supply voltage and a node [forming] , and a protection diode between the power supply line and the node; and

[the] said at least one test pad includes a first test pad connected to a wire that is connected to the power supply line and a second test pad connected to a wire that is connected to the node in the circuit.

5. (Amended) The semiconductor device of claim 1, wherein:

the circuit of the chip IP includes a ground line for supplying a ground voltage and a node [forming] , and a protection diode between the ground line and the node; and

[the] said at least one test pad includes a first test pad connected to a wire that is connected to the ground line and a second test pad connected to a wire that is connected to the node in the circuit.